

**CDS-20**  
**Clock Distribution System**  
**Technical Manual**

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**Revision C**

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# SECTION 1

## DESCRIPTION OF EQUIPMENT

### 1.1 INTRODUCTION

This manual provides general and detailed information on the installation and operation of the Model CDS-20 Clock Distribution System. Section 1 contains a general description of the equipment. Section 2 contains installation instructions. Section 3 contains operating instructions. Section 4 provides the theory of operation. Section 5 contains maintenance and troubleshooting information. Figure 1 is an overall view of the Model CDS-20 System.

### 1.2 DESCRIPTION OF EQUIPMENT

#### 1.2.1 Functional Characteristics

The Model CDS-20 Clock Distribution System in its standard configuration generates 155 different clock frequencies and has the ability to distribute up to 84 different frequencies at one time. The CDS-20 may be used with external reference oscillators to provide frequencies with typical stability of one part in  $10^{12}$  (Stratum I) or with an internal oscillator providing a frequency stability of one part in  $10^8$  (Stratum III). Table 1 lists the frequencies available with the standard line driver cards, and Table 2 lists optional frequencies available with special line driver/synthesizer cards. Many different configurations are possible with the CDS-20 components, and full redundancy is easily realized.

Figure 2 illustrates a typical setup of the CDS-20 using external references. Three separate oscillators are used to provide a triplicate reference input to the system. The user's choice of reference input(s) dictates the choice of reference module (RM) component in the CDS-20. RMs are available that accept inputs at frequencies of 4.0 or 56 KHz, 1.0, 1.544 or 5.0 MHz and with multiple input impedance choices. An internal reference module (IRM) is also available. The reference inputs are applied to each of three separate master divider (MD) cards. A CDS-20 will operate with one, two or three RMs and one MD. True redundancy is achieved with three MDs, however, due to the fact that each MD contains voting logic circuitry for selecting the strongest reference signal. With only two MDs, the two cards keep switching their outputs to the bus, which can cause clock slips that may be noticeable to connected equipment that has a very tight clock tolerance. The voting logic also automatically removes a card from the base frequency bus if an error is detected. Each of the MDs generates the 21 base frequencies that are distributed via a data bus to one to fourteen line driver (LD) cards. Each LD card selects any one of the 21 base frequencies, further divides that frequency to produce eight sub-frequencies, and provides 6 balanced or 12 unbalanced outputs via a DB25F interface. Table 3 lists the characteristics of all of the CDS-20 component modules.

The CDS-20 uses a fully duplicate power system. The two primary supplies convert 110 VAC to 16 VAC that is then distributed to dual power supply circuits on each card. Each circuit is separately fused, and provides DC voltages as required by the circuit card. The two AC power supplies may be replaced with DC-to-AC converters so that the CDS-20 may be operated from a +24 or +48 VDC source. Additionally the system may be operated with one AC and one DC supply. A loss of one primary supply and/or regulator has no effect upon operation of the CDS-20. However, an audible alarm activates and remains on with the loss of the primary supply.



**Figure 1. The CDS-20 Clock Distribution System**

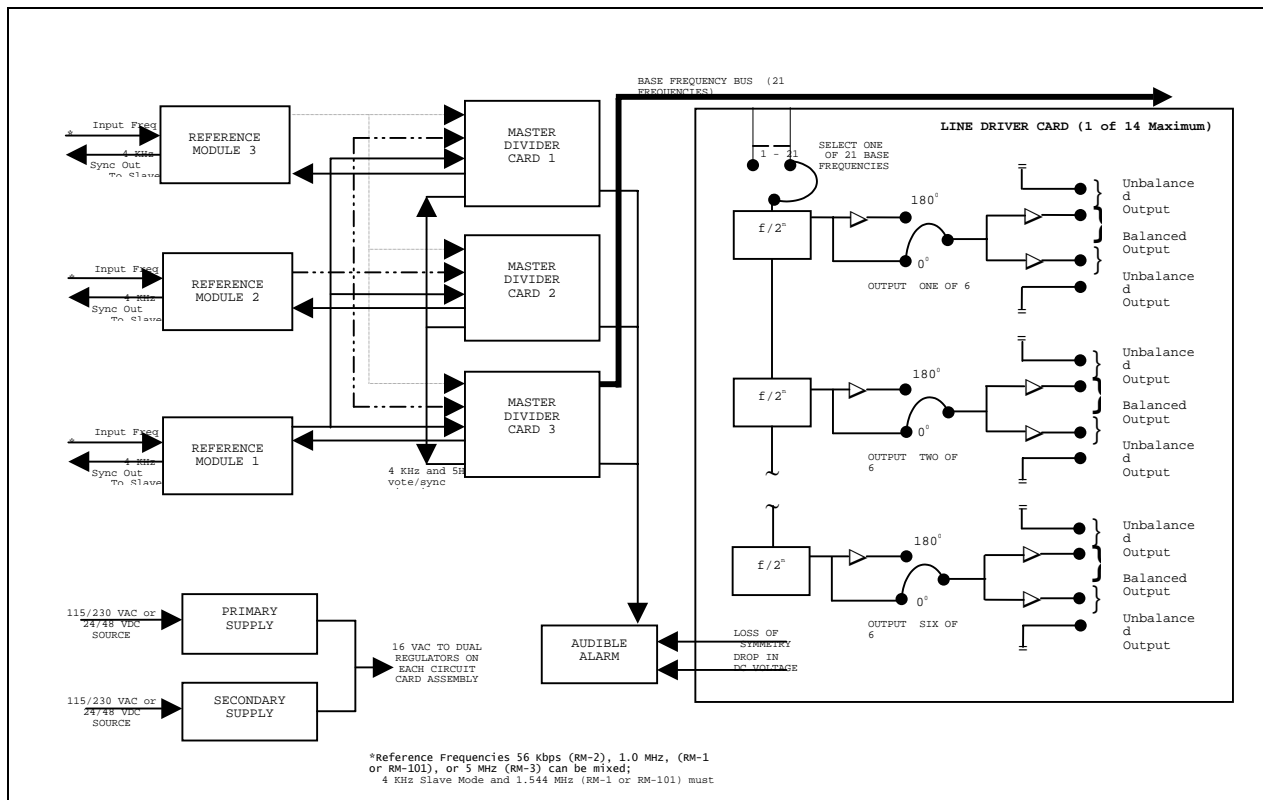
Bus Channel Number	Standard Frequencies (Hz)							
	f	f/2	f/4	f/8	f/16	f/32	f/64	f/128
1	3.072 M	1.536 M	768 K	384 K	192 K	96 K	48 K	24 K
2	2.048 M	1.024 M	512 K	256 K	128 K	64 K	32 K	16 K
3	1.544 M	772 K	386 K	193 K	96.5 K	48.25 K	---	---
4	307.2 K	153.6 K	76.8 K	38.4 K	19.2 K	9.6 K	4.8 K	2.4 K
5	200 K	100 K	50 K	25 K	12.5 K	6.25 K	3.125 K	---
6	120 K	60 K	30 K	15 K	7.5 K	3.75 K	1.875 K	---
7	112 K	56 K	28 K	14 K	7 K	3.5 K	1.75 K	875
8	104 K	52 K	26 K	13 K	6.5 K	3.25 K	1.625 K	---
9	88 K	44 K	22 K	11 K	5.5 K	2.75 K	1.375 K	---
10	80 K	40 K	20 K	10 K	5 K	2.5 K	1.25 K	625
11	72 K	36 K	18 K	9 K	4.5 K	2.25 K	1.125 K	---
12	67.2 K	33.6 K	16.8 K	8.4 K	4.2 K	2.1 K	1.05 K	525
13	64 K	32 K	16 K	8 K	4 K	2 K	1 K	500
14	62.4 K	31.2 K	15.6 K	7.8 K	3.9 K	1.95 K	975	---
15	57.6 K	28.8 K	14.4 K	7.2 K	3.6 K	1.8 K	900	450
16	52.8 K	26.4 K	13.2 K	6.6 K	3.3 K	1.65 K	825	---
17	43.2 K	21.6 K	10.8 K	5.4 K	2.7 K	1.35 K	675	---
18	24 K	12 K	6 K	3 K	1.5 K	750	375	---
19	8 K	4 K	2 K	1 K	500	250	125	---
20	6.4 K	3.2 K	1.6 K	800	400	200	100	50
21	4.8 K	2.4 K	1.2 K	600	300	150	75	

**Table 1. Available Frequencies from Line Driver (LD-3) Card**

Model	Synthesized Frequencies (Hz)						Outputs
	f1	f2	f3	f4	f5	f6	
LD/S-1	6.176 M	4.632 M	3.088 M	1.544 M	---	---	6 Bal
LD/S-2	6.312 M	3.156 M	1.578 M	789 K	---	---	6 Bal
LD/S-3	5.0 M	2.5 M	1.0 M	500 K	---	---	6 Bal
LD/S-4	921.6 K	460.8 K	230.4 K	115.2 K	---	---	6 Bal or 12 Unbal
LD/S-5	12.928 M	9.696 M	6.464 M	3.232 M	---	---	6 Bal
LD/S-6	3.328 M	1.664 M	832 K	416 K	208 K	104 K	6 Bal or 12 Unbal
LD/S-7	1.92 M	1.92 M*	384 K	384 K*	192 K	192 K*	6 Bal
LD/S-T1	1.544 M						6 Bipolar
LD/S-E1	2.048 M						6 Bipolar

**Table 2. Available Frequencies from Line Driver/Synthesizer (LD/S) Cards**

\* Provides a 180° phase-shifted (inverted) frequency signal.



**Figure 2. CDS-20 Simplified Block Diagram**

Model Number	Part Number	Description
CDC-20	19313	Clock Distribution System chassis
Power Supplies:		
PSAC01	14867	115/230 VAC Power Supply, Input & Output Modules
PSAC02	14865	115/230 VAC Power Supply, Input Module only
PSAC03	14866	115/230 VAC Power Supply, Output Module only
PSDC01	17134	24/48 VDC Power Supply, Input & Output Modules
PSDC02	17132	24/48 VDC Power Supply, Input Module only
PSDC03	17133	24/48 VDC Power Supply, Output Module only
Reference Modules:		
RM1-1	18767-01	1.0, 1.544 MHz in, 600 $\Omega$ BNC connectors in & out
RM1-2	18767-02	1.0, 1.544 MHz in, 50 $\Omega$ BNC connectors in & out
RM101-1	19430	1.0, 1.544 MHz in, 600 $\Omega$ BNC connectors in, Fiber out
RM101-2	19909	1.0, 1.544 MHz in, 50 $\Omega$ BNC connectors in, Fiber out
RM102	18653	1.0, 1.544 MHz in, Fiber in, BNC connectors out
RM2	14928	56 KHz in, bal. Terminal strip in, BNC connectors out
RM3-1	17136	5.0 MHz input, 600 $\Omega$ BNC connectors input & output
RM3-2	17137	5.0 MHz input, 50 $\Omega$ BNC connectors input & output
IRM1	14872	1.0 MHz input, 3 BNC sync output connectors
Master Divider:		
MD2-20	19351	Master divider card, 21 frequency output
Line Driver:		
LD-3	15135A	6 bal. or 12 unbal. outputs via DB25F
Line Driver/Synthesizers:		
LD/S-1B	17114	6.176 MHz base frequency, 6 bal. outputs via DB25F
LD/S-2	16250	6.312 MHz base frequency, 6 bal. outputs via DB25F
LD/S-3B	16162	5.000 MHz base frequency, 6 bal. outputs via DB25F
LD/S-4	15890	921.6 KHz base frequency, 6 bal/12 unbal outputs DB25F
LD/S-5B	16941	12.928 MHz base frequency, 6 bal. outputs via DB25F
LD/S-6	17173	3.328 MHz base frequency, 6 bal/12 unbal outputs DB25F
LD/S-7	19513	1.920 MHz base frequency, 6 bal. outputs via DB25F
LD/S-T1	30322-01	1.544 MHz base frequency, 6 bipolar outputs via DB25F
LD/S-E1	30322-01	2.048 MHz base frequency, 6 bipolar outputs via DB25F

**Table 3. Clock Distribution System (CDS-20) Components**

### 1.2.2 Functional Characteristics (cont'd)

The CDS-20 may also be operated as a slave unit. Each RM used in the master unit provides an output synchronization signal that is transmitted via copper or fiber-optic cables to a second CDS-20 (see Figure 2). The slave unit utilizes the same techniques as the master unit to produce clock outputs that have the same frequency stability and are phase coherent with the master clock outputs.

## 1.2.2 Physical Characteristics

The Model CDS-20 Clock Distribution System is designed to be installed in a standard 19-inch rack and requires 7 inches of vertical height. The chassis measures 7.0" (17.8 cm) high x 17.25" (43.8 cm) wide x 18.5" (47.0 cm) deep. The front panel is hinged to provide access to the master divider and line driver cards and the power supply output modules. There are 17 card slots in the CDS-20: the first three (from left to right) are used for MD cards and the remaining fourteen hold the desired number of LD cards. Each MD and LD Port Card measures 5.75" (14.6 cm) high x 0.75" (1.9 cm) wide x 16.5" (41.9 cm) (MD) x 17.13" (43.5 cm) (LD) deep. The LD cards have DB25F interface connectors on the back of the card. The input modules of the power supplies and the reference modules are installed into the rear of the CDS-20 chassis, so that all power and signal connections are made on the rear panel. Most of the RMs have BNC connectors for the reference inputs. Table 3 describes the interfaces for each type of RM. Each circuit card and module of a CDS-20 has a status LED indicator that is ON when the component is operating properly. The power supply output modules also contain audible alarms that are activated when any component LED indicator goes OFF. An interface for remote status monitoring is provided on the power supply input module via a 9-pin D-type connector.

### 1.3 SPECIFICATIONS

**Reference Input Signal:** Sinusoidal or square wave NRZ with a 1 Volt RMS minimum amplitude.

**Reference Input Frequency:** 56 KHz or 1.0, 1.544, or 5.0 MHz, depending on reference module used.

**Reference Input Impedance:** 50, 100 or 600  $\Omega$ , depending on the reference module used.

**Internal Reference:** Optional module to provide a frequency standard, with a 1.0 MHz output and frequency stability of one part in  $10^8$ .

**Output Frequencies:** See Tables 1 and 2 for standard and optional frequencies available.

**Output Stability:** Dependent on the external or internal references; the CDS-20 may be configured to operate with up to 3 separate external references, using a cesium beam, Loran, GPS, or WWV source, for a stability of one part in  $10^{12}$ .

**Output Interface:** Conforms to the requirements of MIL-STD-188-114, balanced or unbalanced; EIA-RS-422, RS-423, and RS-232C. Balanced outputs recommended for frequencies above 1 MHz.

**Output Voltage (LD-3):** +3 VDC balanced, +5 VDC unbalanced.

**Optical Interface (RM-101, RM-102):** ST connectors, compatible with 50/125, 62.5/125 or 100/140  $\mu\text{m}$  fiber-optic cable for 850 nM operation.

**Optical Power Output (RM-101):** -17 dBm.

**Optical Receiver Sensitivity (RM-102):** -33 dB.

**Power Requirements:** Clock Distribution System chassis (CDC-20) is designed to operate with dual redundant power supplies. Power source is 115/230 VAC,  $\pm 10\%$ , 50/60 Hz or 24/48 VDC. Power supplies may require up to 50 watts input, depending on the loading. With dual power supplies on, the typical current draw is 0.3 A and input power is 33 W. With a single power supply, the current draw is 0.45 A and input power is 49.5 W.

**Environment:**  $0^\circ$  to  $+40^\circ\text{C}$  ( $32^\circ$  to  $+104^\circ\text{F}$ ) operating temperature; up to 95% relative humidity (non-condensing); up to 10,000 feet altitude; storage temperature  $-40^\circ$  to  $+70^\circ\text{C}$ .

### 1.3 SPECIFICATIONS (cont'd)

#### Dimensions / Weight:

Component	Height		Width		Depth		Weight	
	(in)	(cm)	(in)	(cm)	(in)	(cm)	(lb)	(kg)
CDC-20	7.0	17.8	17.3	43.9	18.5	47.0	34.0	15.4
RM	1.0	2.5	3.4	8.6	8.13	20.6	0.13	0.06
IRM	3.0	7.6	3.4	8.6	7.0	17.8	1.0	0.45
MD	5.75	14.6	0.75	1.9	16.5	41.9	0.9	0.41
LD	5.75	14.6	0.75	1.9	17.13	43.5	0.75	0.34
PSAC in	1.5	3.8	3.3	8.4	8.13	20.6	0.8	0.36
PSAC out	2.75	7.0	3.2	8.1	7.0	17.8	3.4	1.54
PSDC in	1.5	3.8	3.3	8.4	8.13	20.6	0.9	0.41
PSDC out	2.75	7.0	3.2	8.1	7.0	17.8	2.9	1.33

**Table 4. CDS-20 Component Sizes and Weights**

## SECTION 2 INSTALLATION

### 2.1 GENERAL

This section contains information on the installation and initial checkout of the Clock Distribution System components. Paragraph 2.2 provides instructions for the placement of the chassis. Paragraphs 2.3 through 2.8 contain instructions for connecting the CDS-20 components to the chassis and setting any switches and/or jumpers to configure each component. Paragraph 2.7 describes the output interface for the system. Paragraph 2.9 explains initial checkout procedures.

### 2.2 SITE SELECTION

The Clock Distribution System chassis (CDC-20) is designed for installation into a standard 19-inch rack with four mounting screws. The CDC-20 requires 7 inches of vertical mounting space. Heat dissipation is approximately 100 Watts maximum with a fully loaded chassis. Therefore no special cooling is normally required. All power and signal connections to the chassis are made at the rear so space must be made to accommodate cable requirements. Whenever possible, the CDC-20 should be located so as to minimize cable distances.

### 2.3 POWER REQUIREMENTS

The CDC-20 is designed to operate from an AC power source, a DC power source, or a combination of AC and DC. The unit is 100% redundant so a failure in one of the two supplies will not interrupt operation. Each power supply, whether AC or DC, consists of two separate modules, input and output. The input modules are installed into the horizontal slots provided on the lower right-side rear panel of the CDC-20. Power cords connect to each input module. A DB-9 connector on the input module provides an interface for remote status or control. Table 5 lists the pinouts for this interface. The output modules, which include the power transformer, are installed into horizontal slots on the left side of the inside front of the CDC-20 (i.e., to the left of the circuit card slots). Each output module has two switches, one to set the voltage level input (115 or 230 VAC, or 24 or 48 VDC), and a second switch to set the power supply module for ALARM, MUTE or TEST. This switch is normally kept in the ALARM position.

Pin Designation	Signal Designation	Function
1	-12 V	↑ Operating Voltages for Remote Control / Status Panel
2	- 6 V	
3	Gnd	
4	+6 V	↓ Connection will be made between Normally Open and Common during Alarm
5	+12 V	
6	Normally Open	
7	Common	
8	Normally Closed	
9	Remote Test	Normally High; Gnd will activate Alarm Test

**Table 5. CDS-20 Power Supply Input Module Remote Control Interface**

## 2.4 REFERENCE MODULE INSTALLATION

The CDC-20 may be equipped with one, two, or three external reference modules (RMs), or one internal reference module (IRM). The frequency and input impedance of the external reference(s) you are using determines the particular type of RM used with your application. See Table 3 for a description of the various RMs. The RM circuit cards are installed into the horizontal slots provided on the upper right-side rear panel of the CDC-20, above the power supply input modules. External reference input signals are brought into the CDC-20 via a BNC connector labeled REF on the RM. Each RM also has an output BNC interface, labeled SYNC, which allows for slaving multiple CDC-20s. The RM-101/RM-102 pair uses fiber-optic cable rather than coax for the slaving option. Therefore, the SYNC output of the RM-101 and the REF input of the RM-102 have a ST interface. Further description of the installation of a slave unit is provided in section 2.8. The IRM is exactly the same size as three RMs. It slides into the three RM slots on the upper right-side rear panel of the CDC-20, above the power supply input modules. There are no REF input connectors on an IRM, but it has three SYNC output interfaces with BNC connectors.

## 2.5 MASTER DIVIDER INSTALLATION

**Warning -To minimize contamination of the electrical contacts of the circuit card, avoid touching the card edge contacts located on the right front side of the card. Failure to keep the electrical contacts clean could result in incorrect functioning of the product.**

Opening the Plexiglas front door of the CDC-20 shows the 17 vertical card slots for the MD and LD cards. The first three slots on the left, closest to the power supply output modules, are for the MD cards. Each card is installed by sliding the card into the appropriate slots, electrical contact end first, with the circuit-component side of the card to the right. Slot 1, MD1 card, receives the input reference signal from RM1, located in the highest of the three vertical spaces for RMs on the back panel of the CDC-20. Therefore, if less than three RMs and MDs are used, make certain that the RMs and MDs are installed in the correct slots, i.e., 1 with 1, 2 with 2, etc.

One three-position jumper on the MD circuit card must be set prior to installation of the MD into the CDC-20. Holding the MD with the circuitry facing you (LEDs in upper left and electrical contacts to the right), the jumper, labeled JP1, is found near the bottom edge of the circuit board and about 4 inches (10.2 cm) in from the electrical contacts on the right edge of the card. The jumper connects two of 6 available pins, so either pins 1-2, 3-4, or 5-6 are connected by the blue, rectangular jumper. This jumper is set according to the frequency of the input reference signal, as described in Table 6.

Jumper Setting	Basis
1-2	Slave - Input is 4 KHz sync signal from another CDS-20
3-4	1.0 MHz – Input is 56 KHz, 1.0 or 5.0 MHz or IRM is used
5-6	1.544 MHz – Input is 1.544 MHz external reference

**Table 6. CDS-20 Master Divider Jumper Settings**

## 2.6 LINE DRIVER INSTALLATION

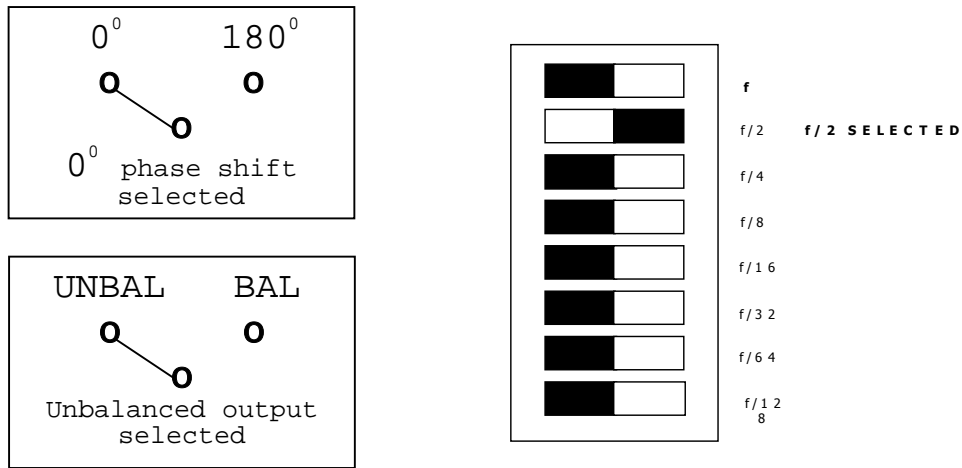
**Warning -To minimize contamination of the electrical contacts of the circuit card, avoid touching the card edge contacts located on the right front side of the card. Failure to keep the electrical contacts clean could result in incorrect functioning of the product.**

Any of the remaining fourteen slots inside the CDC-20 may hold LD or LD/S cards. Like the MDs, each card is installed by sliding the card into the top and bottom slots, electrical contact end first, with the circuit-component side of the card to the right. LD cards provide 6 groups of output circuits, from which 6 balanced or 12 unbalanced output signals are created. When unbalanced outputs are selected, only 6 different frequencies may be chosen, with 2 outputs per frequency possible. The following steps must be taken prior to installing a LD card:

1. First select the base frequency (f) used by the card. On the right side of the circuit card there are 10 rows of three jumper pins plus one more jumper pin below the tenth row. The center row of pins is the data bus, and one of the base frequencies must be connected to the bus with a jumper. The gold-colored metal jumper is inserted so that one of the outlying pins is connected to the bus. There are 21 possible base frequencies (see Table 1 or Figure 3). Figure 3 also shows layout of the jumper pins.
2. Next the setting of balanced vs. unbalanced output and in-phase vs. inverted-phase outputs is selected. The LD card contains 6 groups of circuitry, so these settings are made for each group. There are two sets of three jumper pins within each circuit group, arranged across the middle of the circuit card. The upper set of jumper pins is used to set the phase of the outputs from that circuit group. For in-phase ( $0^\circ$ ) outputs, the upper-left pin must be connected to the center pin with the gold-colored metal jumper. An inverted-phase ( $180^\circ$ ) output is created when the upper-right pin is connected to the center pin. Under the phase-setting pins is a second set for selecting balanced or unbalanced outputs. The pins are laid out the same way, with the unbalanced-setting pin in the upper-left and the balanced-setting pin in the upper right. Figure 4 shows the layout of these jumper pins.

3.072 M	o	o	o	2.048 M
1.544 M	o	o	o	307.2 K
200 K	o	o	o	120 K
112 K	o	o	o	104 K
88 K	o	o	o	80 K
72 K	o	o	o	67.2 K
64 K	o	o	o	62.4 K
57.6 K	o	o	o	52.8 K
43.2 K	o	o	o	24 K
8.0 K	o	o	o	6.4 K
	o			
		4.8 K		
80 KHz BASE FREQUENCY SELECTED				

**Figure 3. CDS-20 Line Driver Base Frequency Settings**



**Figure 4. CDS-20 Line Driver Output Settings**

## 2.6 LINE DRIVER INSTALLATION (Cont.)

3. Lastly, select the LD output frequencies. Once again, the LD card contains 6 groups of circuitry, so these settings are made for each group. There is an 8-position switch for each circuit group, arranged across the upper middle of the circuit card, and above and to the left of the two jumper sets. Each output circuit group may select the base frequency (**f**) or any one of seven sub-multiples (**f/2** through **f/128**). The switch unit is installed with switch position 1 at the top and position 8 at the bottom, with the switches OFF to the left and ON to the right. The switch units and the individual switches are clearly labeled. Turning ON one of the switches selects the output frequency for that circuit group. The 8-position switch is also shown in Figure 4.

## 2.7 CLOCK OUTPUT INTERFACE

Each LD and LD/S card contains one DB25F connector, which is accessible from the rear of the CDC-20. All clock outputs generated by the LD circuitry are available via this DB25. The user must provide the proper connector and cabling for the clock outputs. The interface connections (DB25F pinout) are listed in Table 7. For balanced outputs, connections should be made between each two connector pins (1&2, 3&4, etc.). For unbalanced outputs, connections should be made between each output circuit pin and the corresponding signal ground pin (1&14, 2&15, etc.).

The maximum recommended cabling distance for the clock outputs is dependent on whether balanced or unbalanced outputs are chosen, the clock frequency, and the type of cable used. Table 8 lists distances for various sizes of twisted pair, unshielded cable. For clock rates in excess of 100 KHz balanced transmission via low-loss twinax cable is recommended.

DB-25F Pin Number	Signal Designation	Connection Notes
1	Output Circuit 1	For unbalanced outputs, connection should be made between each output circuit pin and the corresponding signal ground (1&14, 2&15, etc.).
2	Output Circuit 2	
3	Output Circuit 3	
4	Output Circuit 4	
5	Output Circuit 5	
6	Output Circuit 6	
7	Output Circuit 7	For balanced outputs, connection should be made between each two output circuits pins (1&2, 3&4, etc.).
8	Output Circuit 8	
9	Output Circuit 9	
10	Output Circuit 10	
11	Output Circuit 11	
12	Output Circuit 12	Signal Ground for unbalanced circuits 1 through 12, respectively.
13	Not Used	
14-25	Signal Ground	

**TABLE 7. CDC-20 OUTPUT INTERFACE CONNECTIONS**

<b>BALANCED OUTPUTS</b>			
Output Clock Frequency	Twisted Pair Wire Gauge	Maximum Recommended Distance (M / Ft.)	
10 KHz	22	1829	6000
10 KHz	24	1829	6000
10 KHz	26	1829	6000
100 KHz	24	762	2500
100 KHz	26	762	2500
1 MHz	26	305	1000
<b>UNBALANCED OUTPUTS</b>			
10 KHz	22	610	2000
10 KHz	24	610	2000
10 KHz	26	610	2000
100 KHz	24	305	1000
100 KHz	26	305	1000
1 MHz	26	152	500

**TABLE 8. CDC-20 OUTPUT CABLE DISTANCE RECOMMENDATIONS**

## 2.8 INSTALLATION OF A SLAVE UNIT

Two or more CDC-20s may be connected together in a master/slave configuration. The SYNC output from any RM in one CDC-20 may be connected to the REF input of a similar RM in a second CDC-20. This is accomplished for most RMs with a single cable (RG/U-type coax recommended) of up to 0.6 Km (2000 ft.) length with BNC connectors. If the RM-101 is used in the first (master) CDC-20, a single fiber-optic cable of up to 2 Km (6560 ft.) length, with ST optical connectors, is used to connect to an RM-102 in the second (slave) CDC-20. The slave CDC-20 may be equipped with the same combinations of RMs and MDs, e.g., if the master CDC-20 is a triplicate system, then the slave unit should also be triplicate with all three SYNC outputs connected.

**Note: In the slave CDC-20 unit, the RM receiving the REF input must be in the same slot as the MD card for the 4 KHz sync signal to pass correctly between the two units.**

In addition to correctly equipping the slave CDC-20, the MD cards in the slave unit must be set to the SLAVE position, expecting the 4 KHz input, as discussed in Section 2.5.

## 2.8 INITIAL CHECKOUT PROCEDURE

The Clock Distribution System contains no power on/off switch. Once you install and apply power to the unit, it is fully operational. Before beginning system operation the following items should be checked to verify proper installation:

1. Verify that the power supplies are operational in the Clock Distribution System chassis. Set the ALARM/MUTE/TEST switch on one of the power supply output modules to the TEST position. An alarm should be ON. Return the switch to the ALARM position. Repeat this procedure for the second power supply.
2. Verify that the LED indicator is illuminated for each MD and LD card in the chassis. This indicates that the system is in sync and operating properly. A complete description of the operational indicators is found in Section 3. Verify that the switch settings on the MD and LD cards are correct for your configuration.
3. If the CDS-20 is to be used in a master/slave configuration, repeat steps 1 and 2 for the other unit(s). Ideally the same numbers of RMs and MDs are used at both the local and remote Clock Distribution System locations, in the same slot in each chassis. Verify that the coax or fiber-optic cable is connected properly from the SYNC outputs of the first unit to the REF inputs of the second unit. Also confirm that the MD cards are properly set for "SLAVE" operation in all slave units.

If a malfunction is detected during the initial checkout procedure, refer to Chapter 5 for information on isolating the malfunction in the unit.

## **SECTION 3 OPERATION**

### **3.1 INTRODUCTION**

This chapter contains a description of the operating controls and indicators associated with the Model CDS-20 Clock Distribution System. Once the Model CDS-20 is installed and the desired frequencies selected, it is designed to operate on a continual basis without operator intervention. The CDS-20 provides a complete and continuous display of the operating status through the use of LED indicator lamps. All LEDs are ON when the associated circuitry is operating properly.

### **3.2 STATUS INDICATORS / AUDIBLE ALARM**

There are four types of indicators associated with the CDS-20. These include status lamps on the reference input/output modules (RMs), the master divider (MD) cards, the line driver (LD) cards and the power supply input and output modules. Each LED indicator provides a positive indication - when the lamp is ON, the associated circuitry is functioning within the established operational requirements. The MD, LD and power supply output module LEDs are visible through the translucent front panel of the CDC-20. The RM and power supply input module LEDs are visible on the rear of the CDC-20. Figure 5 provides a functional diagram of the alarm circuitry including the status lamps.

The 9-pin connector on the power supply input module may be used as an interface point for a remote status panel. The interface signals available at the connector include normally open and normally closed alarm contacts, an alarm test input, and  $\pm 6$  and  $\pm 12$  volt outputs. The connector pin numbers and signal designations are listed in Table 5 in Section 2.3.

#### **3.2.1 Power Supply Input Module Alarm**

The LED indicator on the power supply input module, visible from the rear of the unit, should be continuously ON. A drop in the  $\pm 6$  volt operating power supplied to the remote connector will cause this indicator to go OUT and will activate the audible alarm.

#### **3.2.2 Power Supply Output Module**

The LED indicator on the power supply output module, visible through the front panel of the unit, should be continuously ON. A drop in the  $\pm 6$  volt operating power supplied to the remote connector will cause this indicator to go OUT and will activate the audible alarm.

#### **3.2.3 Reference Input / Output, Internal Reference Modules**

The LED indicators on these modules, visible from the rear of the unit, should be continuously ON. This indicates that a reference signal is present and being supplied to the master divider circuit(s). If a signal is not present the LED indicator will go OUT and will activate the audible alarm.

PS In status lamp ON indicates that a power input is present and that +6 Volt and -6 Volt signals are present at the remote interface connector

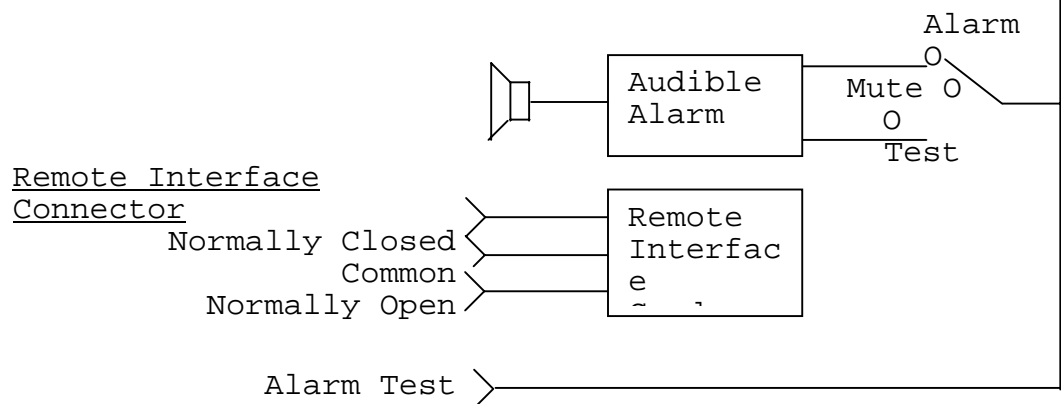
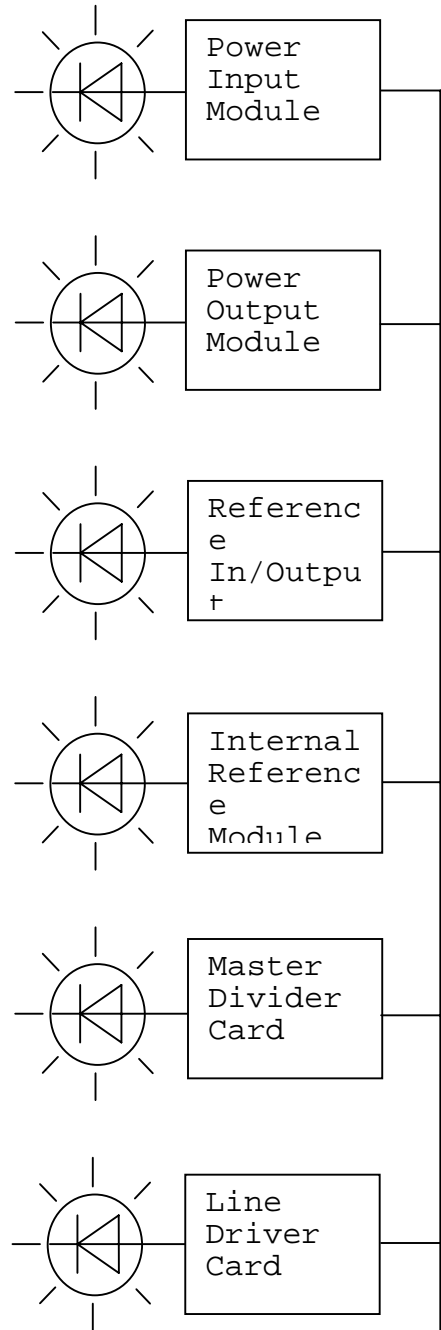
PS Out status lamp ON indicates that AC power input is being sent to the master divider and line driver cards, and that the alarm switch is set to ALARM position

RM status lamp ON indicates that an external reference signal is present and that the signal is being sent to the master divider.

IRM status lamp ON indicates that the oscillator is operating and that the signal is being sent to the master divider.

MD status lamp ON indicates that all four fuses are continuous and both power circuits are operational. All phase lock loops are in lock. In a triplicate system, it also indicates that the reference input and generated frequencies

LD status lamp ON indicates that all four fuses are continuous and both power circuits are operational. A base frequency is present and all stages of the main divider are operating



**FIGURE 5. CDS-20 ALARM CIRCUITRY FUNCTIONAL DIAGRAM**

### **3.2.4 Master Divider Card Alarm**

The LED status indicator on the MD card will go out: 1) if a discrepancy is detected in the frequency of the three reference input signals; 2) if the base frequencies generated on the card are not phase coherent; or 3) if one of the two power circuits on the card fail. The audible alarm, located in the power supply output module, will also be activated when the status indicator goes OUT.

In a triplicate system, a voting discrepancy in one of the cards will cause the card to remove its base frequencies from the output bus and activate the alarm while the other cards continue to operate. If all three cards are in disagreement, then two of the cards will activate the alarm and remove their outputs from the bus while the third card continues operation.

### **3.2.5 Line Driver Card Alarm**

The LED indicator on the LD card will go out: 1) if a loss of symmetry in the output frequency occurs; or 2) if one of the two power circuits on the card fail. The audible alarm, located in the power supply output module, will also be activated when the status indicator goes OUT.

## **3.3 OPERATING CONTROLS**

The only operating controls associated with the CDS-20 are those used to select the base frequencies and the output settings, as discussed in Sections 2.5 and 2.6. The selections that can be made with these switches and jumpers are normally done only at the time of installation. Further changes are not required unless the system requirements change.

## **SECTION 4 THEORY OF OPERATION**

### **4.1 INTRODUCTION**

The Model CDS-20 Clock Distribution System uses reference signals, such as provided by a cesium beam, Loran, GPS or WWV source, to generate and distribute accurate clock frequencies. In most large data communications centers the ability to combine the outputs of several different communications devices is a standard requirement. In order to accomplish this the clocks from each device must be phase coherent. This may be achieved using output buffers to compensate for any remote clock or transmission-induced drift, and by using a master clock to provide simultaneous timing to each of the devices.

The CDS-20 provides a master clock that has versatility, accuracy, reliability and a variable capacity. The standard compliment of LD cards provides a total of 155 different frequencies from 50 Hz to 3.027 MHz, plus additional "special purpose" frequencies are available via LD/S cards. A configuration using three separate external reference signals provides stability of up to one part in  $10^{12}$ . The CDS-20 modular design permits flexible capacity, from a minimum of 6 balanced or 12 unbalanced outputs to a maximum of 84 balanced or 168 unbalanced outputs. This capacity adds to increased reliability through redundancy. For smaller systems, where full redundancy is not practical, the downtime may be kept to a minimum by stocking spare modules. The built-in alarms and modular construction of the CDS-20 results in a mean-time-to-repair of less than two minutes.

The function of each module of the CDS-20 will be described in the following paragraphs.

### **4.2 POWER SUPPLIES PSAC01, PSDC01**

Two power supplies are standard per CDC-20 chassis. Each supply consists of an input and output module. The input module has connectors for the power cord and a DB9 connector for remote alarm. The 115/230 VAC or 24/48 VDC input is transformed by the output module to 16 VAC and is passed to dual regulators on each circuit card assembly installed in the chassis.

### **4.3 REFERENCE MODULES RM-x, IRM**

The RM-1 module buffers 4 KHz, 1.0 MHz, or 1.544 MHz input signals and then transmits them to the bus. The module receives a 4 KHz signal back from the bus, which becomes the SYNC output at the BNC interface, for use as an input to a second CDS-20. The RM-101 is the same as the RM-1 except that the SYNC output is converted to light for transmission via a fiber-optic cable. The RM-102 has a fiber-optic reference (REF) input, but the same 4 KHz SYNC output as the RM-1. Up to three of the RMs may be used per CDC-20 chassis, and they may each be different, i.e., each receive a different reference frequency.

The RM-2 module buffers a 56 KHz input signal into a phase-lock-loop (PLL), voltage-controlled oscillator (VCO), and the output is divided down to 8 KHz. This output is applied to another PLL, 2.0 MHz VCO, divided by two, and applied to the CDC-20 bus as a 1.0 MHz signal. An RM-2 also receives a 4 KHz signal back from the bus, which becomes the SYNC output at the BNC interface, for use as an input to a second CDS-20.

### **4.3 REFERENCE MODULES RM-x, IRM (Cont'd)**

The RM-3 module buffers a 5.0 MHz input signal, divides it down to 1.0 MHz and then transmits it to the bus. It receives the 4 KHz SYNC signal for output via the BNC connector. One to three modules may be used in a system.

The IRM uses an oscillator to create a stable 1.0 MHz reference signal and transmits it to the chassis bus. The IRM has a frequency stability of one part in  $10^8$ . It also receives the 4 KHz signal from the bus and produces 3 SYNC outputs, as the IRM replaces three RMs.

### **4.4 MASTER DIVIDER MD2-20**

The MD card accepts 1-3 reference frequencies from the bus and applies them to a clock recovery circuit to derive the best (most stable) reference. The reference frequency may be 4 KHz, 1.0 MHz or 1.544 MHz. This signal is divided down to 4 KHz and applied to the master oscillator, which creates an output of 12.288 MHz. Through the use of PLL and VCO circuitry, twenty-one base frequencies, from 4.8 KHz to 3.072 MHz, are created and sent to the chassis bus for use by the LDs. Some of the base frequencies are created directly by division of the 12.288 MHz master oscillator output, and others use the 4.8 KHz and 8.0 KHz frequencies, which are also used throughout the MD card for PLL circuitry.

### **4.5 LINE DRIVER LD-3, LD/S-x**

The LD-3 card receives all of the 21 base frequencies from the CDC-20 bus. The LD-3 contains 6 sets of frequency divider circuitry to obtain the specific frequencies desired for output from the system. The phase and the protocol (balanced or unbalanced) of each output are controlled by the LD-3. The LD/S cards use the 4.8 and 8.0 KHz base frequencies to create new frequencies with VCO/PLL circuitry. All line driver cards provide output signals via DB25 connectors.

## SECTION 5 MAINTENANCE AND TROUBLESHOOTING

### 5.1 INTRODUCTION

This chapter contains general information designed to isolate a malfunction in the CDS-20 to a replaceable circuit card or module. The CDS-20 may be equipped with triplicate RMs and MDs, and dual power supplies. Therefore, a failure in one module would not interrupt service. The LD cards do not provide redundancy. However, a failure of an LD card would only affect circuits connected to that card and not the entire CDS-20.

### 5.2 FAULT ISOLATION

The MD and LD cards, and power supply input modules have status indicator LEDs that remain ON to indicate trustable operation. If a malfunction occurs, the LED will go OUT and the audible alarm will activate. Note that with the exception of the power output module, an alarm condition on any one of the modules or cards will cause the associated status indicator to go out and activate the alarm (See Figure 5). The LED on the power output module monitors the AC power applied to the MD and LD cards, and also provides a visual indication that the audible alarm switch is not set to the ALARM position. The alarm circuitry may be checked at any time by setting the switch to the TEST position or by activating the alarm test signal from the remote control panel. The alarm relay contacts are also available at the remote interface connector on the power input module.

**Note: The MD and LD cards are continually comparing the phase of the generated clock signals. Therefore, these cards may generate an alarm condition from a transient error. If this occurs, the clock circuits will resynchronize (typically within one minute) and remove the error condition.**

If the audible alarm remains on for more than one minute, the circuit card or module causing the alarm (with status LED OFF) should be assumed at fault. Turn off the alarm, remove the faulty card or module, reinstall that card or module and recheck the alarm. Once a malfunction is isolated to a particular card or module, check the settings and fuses on the faulty component. Next replace, if possible, the faulty card or module with one known to be functioning properly. Contact VERSITRON Customer Service for assistance for repairs or ordering replacements. Reference the Warranty Statement located in the beginning of this manual for contact information.